

# FE-D Testing and Interface Issues

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## Changes in FE-D from the user's point of view

- Summary of features and interface changes
- Corresponding upgrades of PLL firmware and PixelDAQ software

## First proposal for FE-D testing:

- Initial wafer probing
- Single-chip assembly testing
- Irradiation testing

## **How is FE-D different from FE-A/B/C ?**

- The DAC and Global Register have been combined into a single 109 bit register.
- The Command Register is now only 9 bits long. All Enable functions have been moved to the Global Register.
- The Global Register has a rippling parity check which is always operating and checking that there are an even number of 1's in the register. Errors are flagged in the EOE word.
- Column-Enable capability has been added. This uses a single bit per column pair to control three functions. First, the entire Pixel Register for the column pair will be bypassed (shortening the register length by 320 !). Second, the Hitbus for the column pair will be disabled. Third, the horizontal sparse scan across EOC buffers will skip the disabled column pair.
- Self-trigger mode is implemented, in which a L1 accept is automatically generated by the FE chip HitBus, to allow module testing without making 32 connections for HitBus.
- Internal chopper operation has changed. There is now an internal current-switching chopper with a corresponding 8-bit DAC and two ranges. One range covers 0-6Ke and the other 0-60Ke. External chopping is still an option, and can provide a somewhat larger range (but injection still uses single pass transistor).

- Internal generation of VCCD and VTH control voltages for the front-end is now provided with 5-bit voltage DACs. The range (for VDDA=3.0V) is 1.1V to 2.0V in roughly 31 mV steps. External supplies can be used by setting VCCD=0 and VTH=31.
- The chip now produces two error conditions. Previously (FE-B), the only error was “FE WNG0” which was signaled by row=EO in the EOE word. Now, the EOE word can have the values F0 (OK), E1 (EOC buffer overflow), E2 (parity error) or E3 (both errors).
- The SYNC pin now can act as a synchronous programmable reset pin. Short SYNCs activate the internal SYNC (reset\_FIFO), longer SYNCs activate the SoftReset (reset\_readout), and still longer SYNCs activate the HardReset (reset\_registers). SYNC resets the trigger FIFO pointers (if there are no pending triggers, no data is lost), SoftReset returns the readout logic to an “empty” state, and HardReset resets the Global Register to all zero’s (all DACs are cleared, and all columns are disabled).

## Register Bit Definitions:

- All registers are written with the MSB clocked in first and the LSB clocked in last.  
The LSB is labeled as bit #0, and corresponds to a value of 1 for a bit field.

- The Command Register bits are (LSB = Command(0) = SoftReset):

Command(0) = SoftReset

Command(1) = ClockGlobal: enable CCK to clock DI into the Global Register serial input when LD goes high.

Command(2) = WriteGlobal: transfer data from shift register input into the real latches of the Global Register.

Command(3) = ReadGlobal: transfer data from the latches of the Global Register to serial input register.

Command(4) = ClockSelect: enable CCK to clock DI into Pixel Register when LD goes high.

Command(5) = WriteTDAC2: transfer data from Pixel Register into TDAC2 latch inside pixel control section.

Command(6) = WriteMask: transfer data from Pixel Register into Mask latch inside pixel control section.

Command(7) = WriteTDAC0: transfer data from Pixel Register into TDAC0 latch inside pixel control section.

Command(8) = WriteTDAC1: transfer data from Pixel Register into TDAC1 latch inside pixel control section.

- The Global Register bits are (LSB = Global(0) = EnableCol0):

Global(0:9) = DAC0 block, consisting of (iTuneDac, Bit0, EnableCol0)  
 Global(10:19) = DAC1 block, consisting of (lDDac, Bit1, EnableCol1)  
 Global(20:28) = DAC2 block, consisting of (lFDac, EnableCol2)  
 Global(29:38) = DAC3 block, consisting of (lPDac, Bit2, EnableCol3)  
 Global(39:48) = DAC4 block, consisting of (lLDac, Bit3, EnableCol4)  
 Global(49:58) = DAC5 block, consisting of (lPSDac, Bit4, EnableCol5)  
 Global(59:67) = DAC6 block, consisting of (lChopperDac, Bit5, EnableCol6)  
 Global(68) = EnableCol7  
 Global(69) = EnableCol8  
 Global(70) = Analog Output Enable for test pixel buffer  
 Global(71) = Enable Digital Injection  
 Global(72:74) = Set sense amp bias. The minimum value (0) provides a bias of 1/8 nominal. Each additional increment adds 1/4 of the nominal bias, giving a full-scale value of 1.875 nominal.  
 Global(75:79) = VTH DAC setting (note the bit order for this DAC is inverted!)

Global(80-84) = VCCD DAC setting.

Global(85-86) = Chopper control:

- \* 0 = test (internal Vhigh available on VCal pin)
  - \* 1 = external VCal
  - \* 2 = internal high range (full scale about 60Ke)
  - \* 3 = internal low range (full scale about 6Ke)

Global(87:93) = Gray Generator Latency. A value of 0 corresponds to a latency of 128 crossings.

Global(94:98) = Hitbus self-trigger control, consisting of (Enable, Width(0:3)), where Enable is the MSB, and width controls the number of contiguous L1 accepts. The width should be non-zero, and 1 will generate one L1.

Global(99:102) = DO MUX, the 16:1 multiplexor which controls the routing of the output data to the DO pin.

- \* 0 = register clock (CCK sent to Global Register when ClockGlobal is set)
- \* 1 = Hitbus

- \* 2 = parity\_warning (Global Register parity check result)
- \* 3 = serial\_data (output from serializer)
- \* 4 = L1 accept
- \* 8 = serial\_data
  - \* 9 = command\_output (output from Command Register)
  - \* 11 = pixel\_output (output from Pixel Register)
  - \* 15 = global\_output (output from Global Register)

Note that the outputs 0-7 are "direct" (not synchronized with XCK) whereas 8-15 are synchronized with XCK.

Global(103:106) = MonHit MUX, consisting of the same inputs as the DO MUX, but connected to the MonHit pin.

Global(107:108) = speed control for the column clock generator.

- \* 0 = 20 MHz
- \* 1 = 10 MHz
- \* 2 = 5 MHz
- \* 3 = 5 MHz

## **Interface Issues:**

### **Issues for operating with existing MCC:**

- Current MCC does not support SYNC length control, so cannot provide SYNC\_SoftReset and SYNC\_HardReset.
- Current MCC expects there to be no useful information in the EOE WNG flag (“En”). Hence, such “EOE not equal to F0” events are counted as MCC-WNG errors but the bits that define whether the error was a buffer overflow or a parity error are overwritten.
- Current MCC does not support self-trigger mode. This is a mode in which data is returned from the FE chips on a module without the presence of an MCC-generated trigger to “generate” the data.

### **Issues for operating with existing PLL:**

- Need to add support for SYNC length control (only possible in transparent mode).
- Need to allow self-trigger operation (only in single chip and transparent mode).

### **Upgrades to PixelDAQ:**

- Clearly need to provide support for all of the changes itemized previously.
- A first pass will exist for middle to late October to begin testing. It will be checked using Verilog model of FE-D, and will be used for initial wafer probing.

## Initial Testing Proposal

### **Goal: test two wafers as quickly as possible and get them to Alenia and IZM for bump-bonding:**

- Do not dice any wafers before bumping, since there will only be eight in total, with about 1000 potentially good die.
- Carry out initial tests with PixelDAQ, supplemented to allow DAC characterization using a GPIB scanning ADC. If all goes well, may not need lower level testing.
  - If there are any problems, we will have to resort to using the 200+ probe points Peter placed on FE-D, and verify where problems occur.
- Add some additional pattern testing capability using the digital injection mode to try to obtain good coverage of storage cells (pixel RAM/ROM and EOC buffers) within the PixelDAQ framework.
- Expect DMILL yield to be much lower than HP, so it is important to have good coverage tests to see if chips suffer from small numbers of isolated defects. The FE-B experience was that once a die tested OK at all, it was essentially perfect (all channels worked with digital and analog injection). This is unlikely to be true with the rad-hard chips.
- **Two possibilities:** either John and I go to Bonn for a week in October and we do the testing in one place, or we do the work in parallel in Bonn and LBL. We prefer the latter, with frequent phone calls, etc. to deal with surprises and confusion.

## Can continue to use identical single-chip support cards:

- Have 50 new cards at LBL, and also Bonn and Genova have design files and can (or have already ?) manufacture them independently.
- Once initial two wafers are bumped, some bare die and single-chip assemblies can be attached to these cards for lab and testbeam characterization.

## Other wafers to be tested and bumped after first lab results

- First two FE-D wafers should keep us busy for a while.
- Assume that immediate module development needs can continue to be largely served by the remaining FE-B wafers (there are still a few more to go)
- If all goes well, we may need to consider ordering supplemental wafers in early Spring in order to produce significant numbers of rad-hard modules and continue debugging the rest of the production sequence...

## Designing new **rad-hard single-chip card**:

- This card will use Laurent's buffer chip to replace all radsoft parts on present support card with single DMILL die.
- This card has the same geometry as the present single-chip card, and will allow us to irradiate single chip assemblies and operate them during irradiation.
- It adds 50 ohm buffering for test pixel preamp output.

## Should begin planning **irradiation tests**:

- At LBL, plan to make use of 88" Cyclotron to irradiate single-chip assemblies as soon as possible (Nov or Dec ?)
- In principle, we could do a complete module as well and just replace the non-critical chips on the module support card after irradiation. This would not allow operation during irradiation. Alternatively, we could produce a slightly modified Flex Support Card onto which Laurent's radhard buffer chip could be mounted.
- We should irradiate a Flex module with all passive components, MCC-DMILL test chip, and DMILL DORIC and VDC.
- Attilio is working on preparing for significant PS irradiation next year (see his talk).
- Are there other possible sources of data on irradiated assemblies ???